UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte AVINASH P. CHAKRAVARTHY, BARNES COOPER,
ROBERT GOUGH, and JOHN W. HORIGAN
Appeal 2009-004749
Application 10/251,202
Technology Center 2100

Decided: August 11, 2009

Before ALLEN R. MACDONALD, Vice Chief Administrative Patent Judge,

MACDONALD, Vice Chief Administrative Patent Judge.

DECISION ON APPEAL
Appellant appeals under 35 U.S.C. § 134(a) from the Examiner’s rejection of claims 1-15 and 17-30. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm in-part and enter a new ground of rejection.

STATEMENT OF THE CASE

According to Appellants, the invention relates to an operating system-independent method and system of determining utilization of a CPU within a data processing system.¹

Exemplary Claim

1. A method comprising:
   monitoring clock control signals from a CPU core; and
   calculating a time period during a sampling interval that the CPU core has requested a clock control unit to allow clock signals to be asserted.

9. A method comprising:
   configuring a performance monitor to monitor an event indicating when a clock signal to a CPU core is stopped;
   reading the performance monitor once during a sampling time interval to obtain a value; and
   calculating an effective frequency of the CPU core by dividing the value by the sampling time interval.

27. A device comprising:
   a hardware platform comprising a CPU core, a clock control unit, and a performance monitor to monitor configurable events relating to CPU core performance; and
   a utilization application having privileges to configure the performance monitor to monitor a length of time during a sampling interval that the clock control unit asserts a timing signal based on halt

¹ See Spec. ¶1.
and break signals from the CPU core that cause the clock control unit to respectively start and stop a clock signal to the CPU core, which timing signal indicates a period during the sampling interval during which the clock signal to the CPU was started, and wherein the utilization application calculates a utilization of the CPU core based on the length of time.

Prior Art

The Examiner relies on the following prior art references to show unpatentability:

Circenis 6,816,809 B2 Nov. 9, 2004

Examiner's Rejections

1. The Examiner rejected claims 1-6 and 17-20 under 35 U.S.C. § 102(e) over Circenis.
2. The Examiner rejected claims 7-15 and 21-30 under 35 U.S.C. § 103(a) as being unpatentable over Circenis.

THE 35 U.S.C. § 102(e) REJECTION OVER CIRCENIS

Claims 1-6 and 17-20

ISSUE

The issue before us is whether the prior art teaches a CPU core that requests a clock control unit to allow clock signals to be asserted.

PRINCIPLES OF LAW

In rejecting claims under 35 U.S.C. § 102, “[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation.” Perricone v. Medicis Pharm.
Corporation, 432 F.3d 1368, 1375 (Fed. Cir. 2005). “Anticipation of a patent claim requires a finding that the claim at issue ‘reads on’ a prior art reference. In other words, if granting patent protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless of whether it also covers subject matter not in the prior art.” Atlas Powder Co. v. IRECO, Inc., 190 F.3d 1342, 1346 (Fed Cir. 1999) (internal citation omitted).

Appellants have the burden on appeal to the Board to demonstrate error in the Examiner's position. See In re Kahn, 441 F.3d 977, 985-86 (Fed. Cir. 2006). Therefore, we look to Appellants' Briefs to show error in the Examiner's proffered prima facie case.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the Examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073 (Fed. Cir. 1988). In so doing, the Examiner must make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17 (1966).

If the Examiner’s burden is met, the burden then shifts to the Appellants to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole and the relative persuasiveness of the arguments. See In re Oetiker, 977 F.2d 1443, 1445 (Fed. Cir. 1992).

ANALYSIS

Claims 1-6 and 17-20

Appellants (1) point to a passage from the Final Office Action where the Examiner found that Circenis discloses "calculating a time period during
a sampling interval that the CPU core was used to perform work based on
the clock control signals" (App. Br. 9 citing Final Rejection 2, para. 4).
Appellants argue that the "Examiner's assertions made in the Final Office
Action[,] with respect to claims 1 and 17[,] are inaccurate," as (1) the claims
do not recite a process of calculating a time period during a sampling
interval that the CPU core was used to perform work based on the clock
control signals, but (2) instead, recite calculating a time period during a
sampling interval that the CPU core has requested a clock control unit to
allow clock control signals to be asserted" (Id.).

The Examiner found that "Circenis teaches that the CPU core
provides a halt signal, and that clock control signals are requested when
monitoring of the halt signal indicates that the CPU is not halted [col. 4,
lines 36-45]." (Ans. 12). Further, the Examiner found that "Applicant
discloses in the Specification that the process by which the CPU core
requests clock control signals to be asserted is performed by monitoring a
CPU halt signal [paragraphs 0021-0022]. Thus, Circenis teaches how the
CPU core uses a halt signal to request clock control signals to be asserted,
substantially as claimed." (Ans. 12-13).

We now turn our attention to the portion of Circenis (i.e., col. 4, ll.
36-45) cited by the Examiner for teaching a CPU core that requests a clock
control unit to allow clock signals to be asserted (See Ans. 4, 12). We find
Circenis teaches an idle indicator 120 that indicates when the CPU 110 is not
idle (See Circenis, col. 4, ll. 36-37). Further, we find Circenis teaches (1)
that some operating systems halt the CPU when the CPU is not processing
commands and a halt (idle) indication may be asserted in a pin, and (2) in
one embodiment a halt idle indicator 120 may be coupled to the pin to read
the halt (idle) indication. (See Circenis col. 4, ll. 41-45). While Circenis teaches halting the CPU, we find that the cited portion of Circenis fails to teach specifically making a request to a clock control unit to allow clock signals to be asserted.

Thus, Appellants have persuaded us of error in the Examiner's finding of anticipation regarding independent claim 1, and claims 2-6 which depend therefrom, and the rejection of claims 1-6 is reversed. Independent claim 17 is commensurate in scope with exemplary claim 1. Thus, for the reasons discussed above with regard to exemplary claim 1, we also reverse the Examiner's rejection of independent claim 17, and claims 18-20 which depend therefrom.

THE 103 (A) REJECTION OVER CIRCENIS

Claims 7-15 and 21-30

ISSUE

The issue before us is whether the prior art teaches (1) calculating an effective frequency for the CPU core by dividing the value by the sampling time interval, and (2) a utilization application that calculates a utilization of the CPU core based on a length of time.

FINDINGS OF FACT

1. The Examiner found that “Circenis teaches combining the busy indication … and the measure of computer system time … to generate a value indicative of processor utilization.” (Ans. 13).
2. The Specification of the present application discloses that "an effective frequency is calculated, wherein EffectiveFreq = Ticks / ElapsedTime." (Spec. ¶38).

ANALYSIS

Claims 7-8

Claims 7-8 depend from independent claim 1. Thus, for the reasons discussed above with regard to exemplary claim 1, we also reverse the Examiner's rejection of claims 7-8 which depend therefrom.

Claims 9-15 and 22-26

Appellants argue "[c]laims 9, 13, 22, and 24 were improperly rejected because Circenis does not disclose calculating an effective frequency of a CPU core by dividing a value by a sampling time interval." (App. Br. 13).

The Examiner found (1) Circenis teaches "calculating [a] utilization ratio based on a time period during a sampling interval that the CPU core was used to perform work by dividing the value by the sampling time interval … [col. 2, lines 13-16].” and “[t]hus, Circenis teaches combining the busy indication [when a clock signal to a CPU core is or is not stopped] and the measure of computer system time [the length of the sampling interval] to generate a value indicative of processor utilization; by definition, a ratio is calculated by division." (Ans. 13).

We agree with the Examiner that Circenis discloses generating a value indicative of processor utilization (see FF 1). However, we find that the cited portion of Circenis relied on by the Examiner does not indicate that
utilization equals or involves the calculation of effective frequency, which the Specification of the present application indicates is equal to Ticks divided by elapsed time (see FF 2).

Accordingly, Appellants have persuaded us of error in the Examiner's conclusion of obviousness regarding independent claim 9, and claims 10-12 which depend therefrom, and the rejection of claims 9-12 is reversed. Independent claims 13, 22 and 24 similarly recite "calculating an effective frequency for the CPU core by dividing the value by the sampling time interval" (App. Br. iii. and v., Claims Appendix). Thus, for the reasons discussed above with regard to independent claim 9, the Examiner's rejection of claims independent claims 13, 22, and 24, and claims 14, 15, 23, 25, and 26, which depend from independent claims 13, 22, and 24, respectively, is also reversed.

Claim 21

Claim 21 depends from independent claim 17. Thus, for the reasons discussed above with regard to independent claim 17, we also reverse the Examiner's rejection of claim 21, which depends therefrom.

Claims 27-30

Appellants contend "[c]laim 27 was improperly rejected because Circenus does not disclose or suggest a utilization application calculating a utilization of a CPU core based on a length of time" (App. Br. 14). Appellants’ arguments with regard to claim 27 also apply to claims 28-30, which depend from independent claim 27 (see App. Br. 15).
As Circenis discloses, a means *(i.e., utilization application)* that utilizes a measure of computer system time to generate a value indicative of processor *(i.e., CPU)* utilization, we agree with the Examiner that Circenis teaches "a utilization application calculates a utilization of the CPU core based on a length of time," as recited in independent claim 27*(See FF 1).* Accordingly, Appellants have not persuaded us of error in the Examiner's conclusion of obviousness regarding independent claim 27, and claims 28-30 which depend therefrom. Thus, the Examiner's rejection of claims 27-30 is sustained.

**OTHER ISSUES**

**NEW GROUND of REJECTION**

*Claims 17-26*

We make the following new grounds of rejection using our authority under 37 C.F.R. § 41.50(b).

Claims 17-26 are rejected under 35 U.S.C. § 101 for being non-statutory. Claims 17-26 recite a computer-readable medium *(see App. Br. iv.-vi., Claims Appendix)*. The Specification of the present application discloses that (1) "a machine-readable medium includes any mechanism that provides (i.e., stores and/or transmits) information in a form readable by a machine (e.g. computer) for example, a machine readable medium includes … acoustical or other form [sic] of propagated signals (e.g. carrier waves, infra red signals, and digital signals)" *(Spec. ¶0040).*

We find the computer-readable medium of claims 17-26 is a machine-readable medium, as defined in the Specification of the present application.
As such, we find the computer readable medium of claims 17-26 may take the form of propagated signals. Such a claim for computer instructions embodied in a signal only is not considered to be statutory under 35 U.S.C. § 101. This policy has recently been confirmed by the Court of Appeals for the Federal Circuit in *In re Nuijten*:

“A transitory, propagating signal like Nuijten's is not a ‘process, machine, manufacture, or composition of matter.’ Those four categories define the explicit scope and reach of subject matter patentable under 35 U.S.C. § 101; thus, such a signal cannot be patentable subject matter.”

*In re Nuijten*, 500 F.3d 1346, 1357 (Fed. Cir. 2007). Accordingly, we reject claims 17-26, under 35 U.S.C. § 101 for failing to recite statutory subject matter.

**DECISION**

We reverse the Examiner's rejection with respect to claims 1-26. We sustain the Examiner's rejection of claims 27-30. Moreover, we enter a new ground of rejection under 37 C.F.R. § 41.50(b) for claims 27-30, as failing to recite statutory subject matter under 35 U.S.C. § 101.

37 C.F.R. § 41.50(b) also provides that the Appellants, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:

1. Reopen prosecution. Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner….
(2) Request rehearing. Request that the proceeding be reheard under § 41.52 by the Board upon the same record.…

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

**AFFIRMED-IN-PART**

37 C.F.R. § 41.50(b)

nhl

INTEL/BSTZ
BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP
1279 OAKMEAD PARKWAY
SUNNYVALE CA 94085-4040